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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,974	10/19/2001	Donald Kane	2070.006800/P6928	8124

23720 7590 07/29/2004

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER

MANOSKEY, JOSEPH D

ART UNIT	PAPER NUMBER
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2113

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/043,974	Applicant(s) KANE ET AL.	
	Examiner Joseph Manoskey	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/25/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 20-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. It is suggested the Applicant changes "An article comprising one or more machine-readable storage media" to "A computer-readable medium".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al., U.S. Patent 6,480,975, hereinafter referred to as "Arimilli".
6. Referring to claim 1, Arimilli teaches a method of detecting errors in data stored in a storage device in a system (See Col. 1, lines 5-12), determining if the error is correctable (See Col. 4, lines 24-26), and making at least a portion of the storage device unavailable to one or more resources in the system in response to determining that the error is uncorrectable (See Col. 6, lines 2-5).
7. Referring to claim 2, Arimilli teaches the use of ECC (error correction code) for detecting the errors (See Col. 4, lines 52-57).
8. Referring to claim 3, Arimilli discloses determining if the detected error is correctable by determining that the detected error is a multi-bit error (See Col. 4, lines 24-26).
9. Referring to claim 4, Arimilli teaches the use of parity checks and including being applied to address tags (See Col. 4, lines 43 and 54-55).

10. Referring to claim 5, Arimilli discloses making at least the portion of the storage device unavailable comprises making at least the portion of the storage device unavailable while the system is in operation (See Col. 6, lines 2-5).

11. Referring to claim 6, Arimilli teaches testing the storage device based on determining that the error is uncorrectable (See Col. 4, lines 25-26).

12. Referring to claims 7 and 8, Arimilli discloses including a retry circuit and allowing ECC to attempt to correct the problem, this is interpreted as servicing the storage device in response to testing and then dynamically allowing access to the storage unit in response to testing the storage device (See Col. 6, lines 2-5).

13. Referring to claim 9, Arimilli teaches the storage device being a directory cache (See Col. 4, lines 54-55). Also, Arimilli teaches halting the operation, this is interpreted as generating a cache miss (See Col. 6, lines 12-14).

14. Referring to claim 10, Arimilli discloses an apparatus comprising a directory cache adapted to store at least one entry (See Fig. 1 and Col. 4, lines 54-55). Also the apparatus includes a cache controller (See Col. 1, lines 58-60). Arimilli teaches determining if an error in the directory cache is uncorrectable (See Col. 4, lines 24-26), and placing the directory cache offline in response to determining that the error is uncorrectable (See Col. 6, lines 2-5).

15. Referring to claim 11, Arimilli teaches the cache being set-associative (See Col. 2, lines 65-67), this interpreted as including three-way set associative.

16. Referring to claim 12, Arimilli discloses determining if the detected error is correctable by determining that the detected error is a multi-bit error (See Col. 4, lines 24-26).

17. Referring to claim 13, Arimilli teaches the use of parity checks and including being applied to address tags (See Col. 4, lines 43 and 54-55).

18. Referring to claim 14, Arimilli discloses cache is associated with a domain, and wherein the control unit places the directory cache offline while the domain is active (See Col. 6, lines 2-5).

19. Referring to claim 15, Arimilli teaches halting the operation, this is interpreted as generating a cache miss while the directory cache is offline (See Col. 6, lines 12-14).

20. Referring to claim 16, Arimilli teaches testing the control unit testing the directory cache based on determining that the error is uncorrectable (See Col. 4, lines 25-26).

21. Referring to claims 17, 18, and 19, Arimilli discloses including a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as servicing the directory cache in response to testing and then dynamically placing the directory cache online in response to testing the storage device (See Col. 6, lines 2-5).

22. Referring to claim 20, Arimilli a cache controller that executes machine-readable instructions (See Col. 1, lines 58-60). Arimilli discloses determining if the detected error is correctable by determining that the detected error is a multi-bit error (See Col. 4, lines 24-26). Arimilli teaches determining if an error in the directory cache is uncorrectable (See Col. 4, lines 24-26), and isolating the directory cache in response the multiple bit error (See Col. 6, lines 2-5).

23. Referring to claim 21, Arimilli teaches the use of ECC (error correction code) for detecting the errors (See Col. 4, lines 52-57).

24. Referring to claim 22, Arimilli teaches testing the storage device in response to isolating the storage device (See Col. 4, lines 25-26).

25. Referring to claim 23, Arimilli discloses including a retry circuit and allowing ECC to attempt the correct the problem, this is interpreted as dynamically restoring the storage unit in response to testing the storage device (See Col. 6, lines 2-5).

26. Referring to claim 24, Arimilli teaches indicating an error has occurred in reading the address tag, this is interpreted as providing a cause of the multiple-bit error (See Col. 5, lines 48-51).

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are examples of closely related cache systems and cache systems with error detection.

U.S. Patent Application Pub. 2003/0028819 to Chiu et al.

U.S. Patent 5,544,341 to Nakagawa et al.

U.S. Patent Application Pub. 2002/0124143 to Barroso et al.

U.S. Patent 6,622,267 to Zhang

U.S. Patent 5,963,718 to Muramatsu

U.S. Patent 5,894,487 to Levitan

U.S. Patent 6,078,995 to Bewick et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone

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number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
July 22, 2004


ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100